REMARKS

This is in response to the Office Action of 04 May 2004. Claims 1 and 3-16 are pending in the application, and Claims 1 and 3-16 have been rejected.

By this Response, arguments traversing all the rejections are presented.

No Claims are amended or cancelled by this Response.

No new matter has been added.

In view of the remarks below, Applicants respectfully request reconsideration, withdrawal of the improper rejections, and further examination.

About The Invention

The present invention relates generally to methods of forming vias to conductive lines, and more particularly relates to such methods wherein the conductive lines have conductive capping layers, silicon carbide etch stop layers over and adjacent to the conductive lines and capping layers, and low-k dielectric material disposed over the silicon carbide etch stop layer.

Comments on Examiner's "Response to Arguments"

The Examiner has provided, in the Office Action dated 04 May 2004, a section entitled "Response to Arguments" in which alleged deficiencies in Applicants' prior filed response are noted.

Applicants respectfully assert that the Examiner is in error regarding the content of Applicants' Claims and arguments. The Examiner states that Applicants argued that the previously cited art does not teach applying an etch stop layer to the conductor sidewall; and further states that this feature was not recited in the rejected Claims. Applicants note that, in fact, Claim 1 was amended in the Response and Amendment of 13 February 2004 to contain the following language:

> wherein the etch stop layer is applied to the top surface portion and the sidewall portions of the conductor after the provision of th conductor at the surface of the semiconductor substrate.

In view of the foregoing, Applicants respectfully ass rt that the f ature of applying an etch stop layer to the conductor sidewall is clearly present in independent Claim 1, and further assert that the Examiner's statement to the contrary is clearly erroneous.

Rejections under 35 USC 102(e)

Claims 1, 3-5, 9, and 12 have been rejected under 35 USC 102(e) as being anticipated by Avanzino, et al. (6,593,632).

Claims 13-14 have been rejected under 35 USC 102(e) as being anticipated by Wolstenholme, et al. (6,649,968).

With respect to Claims 1, 3-5, 9, and 12, Applicants respectfully traverse the rejections under 35 USc102(e), and request that they be withdrawn.

Applicants urge the Examiner to review the recited limitations of independent Claim 1. The limitations set forth in previously presented Claim 1 make clear that the etch stop layer is applied to the top portion and the sidewall portions of the conductor.

Avanzino, et al., do not disclose, suggest, or provide motivation for the invention defined by previously presented Claim 1. The disclosure of Avanzino, et al., does not disclose applying the etch stop layer to the conductor sidewalls. Rather, Avanzino, et al., disclose that the etch stop layer is separated from the conductor sidewalls by a sidewall spacer (Fig. 1, element 20; and column 4, lines 10-12). For at least this reason, Applicants respectfully submit that the rejection of Claim 1 under 35 USC 102(e) is improper and should be withdrawn. Similarly, Applicants submit that the rejections of Claims 3-5, 9 and 12, which depend directly or indirectly from previously presented Claim 1, are also improper and should be withdrawn.

Applicants further respectfully submit, that the inventions defined by Applicants' Claims 1, 3-5, 9, and 12 are not suggested or motivated by the disclosure of Avanzino, t al.

With respect to Claims 13-14, Applicants respectfully traverse the rejections under 35 USc102(e), and request that they be withdrawn.

The disclosure of Wolstenholme has been carefully reviewed, and Applicants respectfully assert that Wolstenholme does not disclose the invention defined by independent Claim 13. More particularly, Applicants' Claim 13 clearly recites that an electrically conductive capping layer is disposed on the top surface of the patterned conductor. The structure of Wolstenholme referred to by the Examiner (i.e., element 23 of Fig. 9) is actually a floating gate. A floating gate by definition is electrically isolated, and therefore does not have an electrically conductive capping layer disposed on the top surface thereof. It is well-known in the semiconductor manufacturing arts that a floating gate is not in contact with any other electrically conductive element. Applicants' claimed process simply cannot produce the structure disclosed by Wolstenholme.

For at least the reasons set forth above, Applicants respectfully submit that the invention defined by independent Claim 13 is not anticipated by Wolstenholme. Similarly, Claim 14, which depends from Claim 13, is also submitted to be distinguishable from Wolstenholme.

Additionally, Wolstenholme, which discloses the formation of flash memory structures, does not suggest or provide motivation for the invention set forth in Claims 13-14.

Rejections under 35 USC 103(a)

Claims 7-8 and 10 have been rejected under 35 USC 103(a), as being unpatentable over Avanzino, et al., as applied to Claims 1, 3-5,9 and 12, in view of Boeck, et al., (US Patent 5,880,018).

Claims 6 and 11 have been rejected under 35 USC 103(a), as being unpatentable over Avanzino, et al., in view of Ngo, et al., (US Patent 6,190,966).

Claim 15 has been rejected under 35 USC 103(a), as being unpatentable over Wolstenholme as applied to Claims 13-14, and further in view of Avanzino, et

al.

Claim 16 has been rejected under 35 USC 103(a), as being unpatentable over Wolstenholme and Avanzino, et al., as applied to Claims 15, and further in view of Boeck, et al.

With respect to Claims 7-8, Applicants respectfully traverse the rejections of these Claims under 35 USC 103(a), and request that these rejections be withdrawn.

As asserted above by Applicants, previously presented independent Claim 1 has been improperly rejected in view of Avanzino, et al., because the recited features of Claim 1 (e.g., applying the etch stop layer to the conductor sidewalls) are not disclosed by Avanzino, et al. Rather, Avanzino, et al., disclose that the etch stop layer is separated from the conductor sidewalls by a sidewall spacer (Fig. 1, element 20; and column 4, lines 10-12). Since Claims 7-8 depend, directly or indirectly, from previously presented Claim 1, the rejection of these Claims based on Avanzino, et al., is defective. Furthermore, the Examiner has incorrectly characterized the barrier layer 64 of Boeck, et al., as the capping layer recited in Applicants' Claims. It is clear that the barrier layer 64 of Boeck, et al., is different from the capping layer illustrated and described in Applicants' patent application (see, for example, elements 8, 9, and 10, in Figs. 1-4). The barrier layer 64 of Boeck, et al., covers only a portion of the conductor top surface, which is inherently not the function of a capping layer. Applicants' use of the expression "capping layer" is well-understood in the semiconductor manufacturing arts to represent a layer that covers a complete surface of a structure, and not only a partial surface of that structure.

Furthermore, the barrier layer 64 of Boeck, et al., does not have its surface covered by the etch stop layer, as is clearly called for by the recitations of Claim 7. In other words, Claim 7 says that the top surface of the conductor is the top surface of the capping layer, while Claim 1 recites that the etch stop layer is on the top surface of the conductor. Clearly, Boeck, et al., do not disclose the features of Applicants' Claims.

In view of the foregoing Applicants respectfully assert that the rej ctions of Claims 7-8 are improper and request that they be withdrawn.

With respect to Claim 10, Applicants respectfully traverse the rejection of this Claim under 35 USC 103(a), and request that this rejection be withdrawn.

As set forth in detail above, Applicants assert that previously presented independent Claim 1 has been improperly rejected in view of Avanzino, et al., because the recited features of Claim 1 (e.g., applying the etch stop layer to the conductor sidewalls) are not disclosed by Avanzino, et al. Since the combination of Avanzino, et al., and Boeck, et al., do not disclose, suggest, or provide motivation for the invention set forth in Claim 10, Applicants request that this improper rejection be withdrawn.

With respect to Claim 6 and11, Applicants respectfully traverse the rejection of these Claims under 35 USC 103(a), and request that this rejection be withdrawn.

Both Claims 6 and 11 depend directly from previously presented Claim 1, which Applicants have shown above is not disclosed, suggested, or motivated by Avanzino, et al. The Examiner cites Ngo, et al., for the disclosure of tungsten in a via opening. Applicants respectfully assert that the combination Avanzino, et al., and Ngo, et al., do not disclose, suggest, or provide motivation for the claimed invention, and therefore this improper rejection should be withdrawn.

With respect to Claim 15, Applicants respectfully traverse the rejection of this Claim under 35 USC 103(a), and request that this rejection be withdrawn.

Claim 15 depends from Claim 14, which Applicant has argued above is not disclosed, suggested, or motivated by Wolstenholme. The Examiner cites Avanzino, et al., for a teaching of the use of silicon carbide as an etch stop layer. However, this combination does <u>not</u> teach, suggest, or motivate the claimed capping layer on the surface of the conductor, and therefore this improper rejection should be withdrawn.

With respect to Claim 16, Applicants respectfully traverse the rejection of this Claim under 35 USC 103(a), and requ st that this rejection be withdrawn.

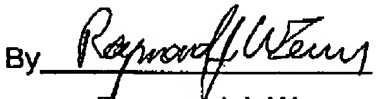
The combination of Wolstenholme, Avanzino, et al., and Boeck, et al., do not disclose, suggest, or provide motivation for the invention defined by Claim 16. More particularly, Applicants have shown that: Wolstenholme discloses a floating gate and not a conductor with a capping layer; Avanzino, et al., disclose an etch stop layer that is separated from the sidewalls of the conductor and not in contact therewith; and Boeck, et al., disclose a barrier layer and not a capping layer. The agglomeration of elements from this combination of references does not produce Applicants' claimed invention, nor do these references in any way suggest or motivate the invention set forth in Applicants' Claims. The improper rejections should be withdrawn.

Conclusion

All of the rejections in the outstanding Office Action of 04 May 2004 have been responded to, and Applicants respectfully submit that the pending Claims 1 and 3-16 are now in condition for allowance.

Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

By 

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Portland, Oregon

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